PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-259159
(43)Date of publication of application : 08.10.1993

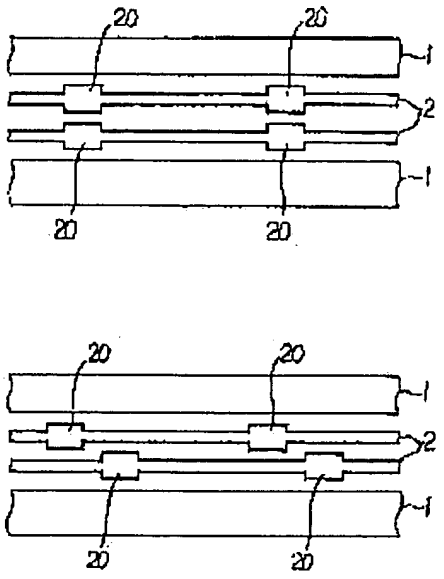
(51)Int.Cl. H01L 21/3205

(21)Application number : 04-058222
(22)Date of filing : 16.03.1992

(71)Applicant : NEC IC MICROCOMPUT SYST LTD
(72)Inventor : WATANABE MASAYUKI

(54) SHAPE OF WIRING IN SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PURPOSE: To minimize the increase in parasitic capacitance produced in a wiring and prevent photoresist from falling on a semiconductor integrated circuit having wirings having constant widths on a semiconductor substrate by making at least one part of the wirings wider than the rest thereof.
CONSTITUTION: A semiconductor integrate circuit device has wirings 1 and 2 having constant widths on a semiconductor substrate. At least one part 20 of the wirings 1 and 2 is made wider than the rest thereof. Or, parts 20 of the wirings 1 and 2 are made wider than the rest thereof with the wider parts 20 of one 2 of the adjacent wirings shifted in position from those of the other in the wiring longitudinal direction. For example, in a wiring pattern 2 of a minimum wiring width, parts are formed 20 with the cross-sectional width approx. 1.5 to 2 times the thicknesses and length several μm lengths at a specified interval. Or, the position of the parts 20 of a larger width is, in addition, shifted in the lengthwise direction.



LEGAL STATUS

[Date of request for examination] 28.03.1996
[Date of sending the examiner's decision of rejection] 17.06.1998
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The wiring configuration in the semiconductor integrated circuit equipment characterized by forming in said some of wiring at least one width-of-face Hirobe set as the predetermined dimension in the semiconductor integrated circuit equipment with which wiring which extends by fixed width of face was prepared on the semi-conductor substrate.
[Claim 2] The wiring configuration in the semiconductor integrated circuit equipment characterized by being prepared in the location where width-of-face Hirobe is formed in said some of wiring, and width-of-face Hirobe of this next door **** wiring shifted in the direction of a wire-length hand in the semiconductor integrated circuit equipment with which wiring which extends by fixed width of face was prepared on the semi-conductor substrate.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to amelioration of the configuration of wiring near especially the minimum wiring width of face about semiconductor integrated circuit equipment.
[0002]
[Description of the Prior Art] The circuit pattern in conventional semiconductor integrated circuit equipment has very many parts set as the fixed size, as shown in drawing 3 and drawing 4 . Especially wiring that connects an active element and an active element is formed over several 100 micrometers thru/or several 1000 micrometers by the fixed width of face defined with the semiconductor integrated circuit equipment.
[0003] The width of face of wiring is determined by factors, such as magnitude of a current, wiring resistance, etc. which flow the wiring. and close to the minimum wiring width of face in that semiconductor integrated circuit equipment, in order that especially this factor may make parasitic capacitance as small as possible about wiring of the signal which does not pose a problem -- it is formed. Or for improvement in a degree of integration, wiring is formed so that the minimum wiring width of face and spacing may be set.
[0004] Moreover, if it says about the thickness of a wiring layer, making a wiring layer thin will make the cross section small, and it will enlarge current density. If it does so, since it will worsen to electromigration, it is the actual condition to try for thickness not to change, even if minimum line width becomes small.
[0005]
[Problem(s) to be Solved by the Invention] Drawing 5 shows the condition after a photoresist 3 carries out patterning. Recently, in order that wiring width of face may use about 0.6-0.8 micrometers, inevitably, as for the thickness, the width of face of a photoresist 3 is determined by the thickness of a wiring layer to 0.6-0.8 micrometers, and the thickness is about 1-3 micrometers. Width of face of 0.8 micrometers shows drawing 5 taking the case of the case with a thickness of 2 micrometers. Thus, the cross-section configuration of a photoresist 3 had become longwise [-like], when extreme, when etching a wiring layer, the photoresist 3 fell, and there was a trouble that even the part which is going to leave the wiring layer under it will be etched.
[0006] This problem is so remarkable that the straight-line part of a circuit pattern is long, and as shown in drawing 5 , when a wiring layer 4 is formed in parallel between two lower layer wiring layers 8, a photoresist becomes thick inevitably with a level difference, the cross-section configuration of a photoresist 3 will become longwise [-like] further, and a problem will remain too.
[0007] Although what is necessary is to enlarge wiring width of face and just to make it a photoresist not fall, in order to prevent this, if it does so, the problem that parasitic capacitance becomes large will arise.
[0008] This invention aims at preventing that it was proposed in view of the technical problem of the above-mentioned conventional technique, and control buildup of the parasitic capacitance attached to wiring to the minimum in the semiconductor integrated circuit with which wiring

which extends by fixed width of face in an one direction was prepared on the semi-conductor substrate, and a photoresist falls.

[0009]

[Means for Solving the Problem] This invention is characterized by preparing a part for at least one width-of-face Hirobe in said some of wiring in the semiconductor integrated circuit with which wiring which extends by fixed width of face in an one direction was prepared on the semi-conductor substrate.

[0010]

[Function] Since wiring width of face is narrowly set up as the whole, said wiring can control buildup of parasitic capacitance and, moreover, can prevent that a photoresist breaks down from the existence for width-of-face Hirobe.

[0011]

[Example] The 1st example of this invention is explained. Drawing 1 is the top view of the 1st example, and two circuit patterns 2 which used the minimum wiring width of face of this invention between the circuit patterns 1 of both sides exist. The width of face of a cross section is set as the about 1.5 to 2 times [of thickness] size, respectively, width-of-face Hirobe 20 by whom die length is set as several micrometers sets predetermined spacing, and these circuit patterns 2 are formed. It is prevented that a photoresist falls by this width-of-face Hirobe's 20 existence.

[0012] Although width-of-face Hirobe 20 formed in the circuit pattern 2 of both minimum line width in the 1st example of the above was formed in the location which faces mutually, if the 2nd example shifts mutually width-of-face Hirobe formed in the circuit pattern 2 of up-and-down minimum line width at a longitudinal direction as shown in drawing 2 , it is located. Both the circuit patterns 2 can be made to approach by this, and it becomes possible to narrow spacing of a circuit pattern 2.

[0013]

[Effect of the Invention] Though buildup of the parasitic capacitance of wiring is controlled to the minimum by preparing width-of-face Hirobe in said some of wiring in the semiconductor integrated circuit equipment with which wiring which extends by fixed width of face was prepared in the one direction on a semi-conductor substrate according to this invention as described above, it becomes possible about a photoresist falling to prevent effectively.

[0014] Moreover, when the width of face to which the photoresist was left behind by the variation on manufacture has become thin, it becomes possible to prevent that a photoresist falls.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The top view having shown the 1st example of this invention.
[Drawing 2] The top view having shown the 2nd example of this invention.
[Drawing 3] The top view having shown the conventional wiring.
[Drawing 4] The sectional view having shown the conventional wiring.
[Drawing 5] The sectional view having shown the condition after the photoresist in the conventional technique carries out patterning.
[Description of Notations]
1 -- Wiring
2 -- Wiring of this invention
3 -- Photoresist after patterning
20 -- Width-of-face Hirobe

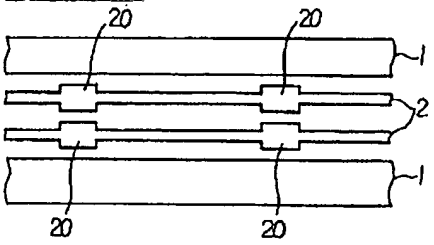
[Translation done.]

* NOTICES *

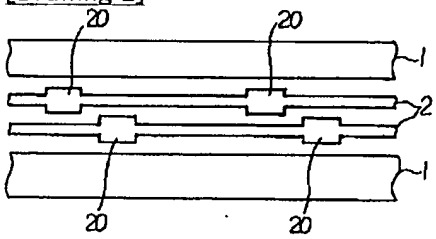
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

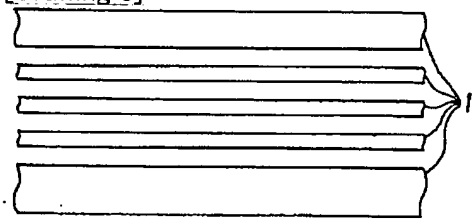
[Drawing 1]



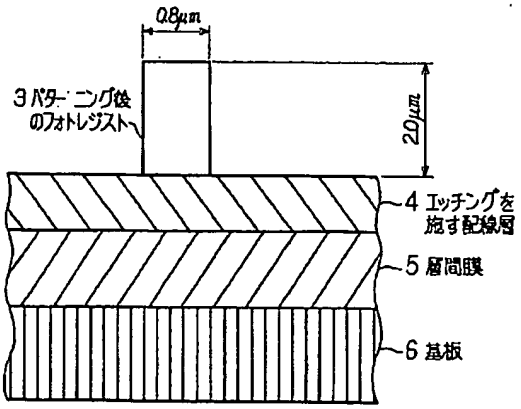
[Drawing 2]



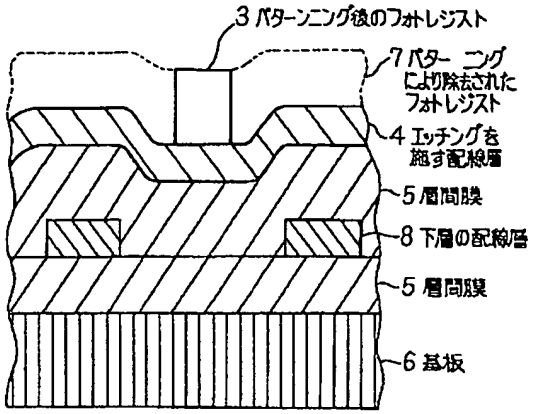
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]

(3-4)

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号

特開平5－259159

(43)公開日　平成５年(1993)10月８日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
H01L 21/3205				
		7735-4M	H01L 21/88	A

審査請求　未請求　請求項の数２　（全３頁）

(21)出願番号　特願平4－58222

(22)出願日　平成４年(1992)３月16日

(71)出願人　000232036
日本電気アイシーマイコンシステム株式会社
神奈川県川崎市中原区小杉町１丁目403番53

(72)発明者　渡邊　正行
神奈川県川崎市中原区小杉町一丁目403番53　日本電気アイシーマイコンシステム株式会社内

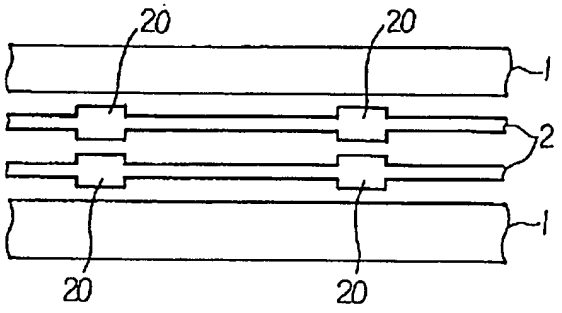
(74)代理人　弁理士　後藤　洋介　（外２名）

(54)【発明の名称】半導体集積回路装置内の配線形状

(57)【要約】

【目的】　半導体基板上に一定の幅で延在する配線が設けられた半導体集積回路において、配線の寄生容量の増大を最小限に抑制し、かつ、フォトレジストが倒れることを防止すること。

【構成】　配線（２）の一部に所定の寸法に設定された幅広部（２０）を少なくとも一つ形成する。



1

【特許請求の範囲】

【請求項１】　半導体基板上に一定の幅で延在する配線が設けられた半導体集積回路装置において、
前記配線の一部に所定の寸法に設定された幅広部が少なくとも一つ形成されていることを特徴とする半導体集積回路装置内の配線形状。

【請求項２】　半導体基板上に一定の幅で延在する配線が設けられた半導体集積回路装置において、
前記配線の一部に幅広部が形成されており、かつ、該隣り合う配線の幅広部が配線長手方向においてずれた位置に設けられていることを特徴とする半導体集積回路装置内の配線形状。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体集積回路装置に関し、特に最小配線幅に近い配線の形状の改良に関するものである。

【０００２】

【従来の技術】従来の半導体集積回路装置における配線パターンは、図３、図４に示すように、一定の太さに設定された部分を非常に多く有している。特に、能動素子と能動素子とを結ぶ配線はその半導体集積回路装置にて定められた一定の幅で数１００μｍないし数１０００μｍにわたって形成されている。

【０００３】配線の幅は、その配線を流れる電流の大きさや配線抵抗などの要因により決定される。そして、この要因が特に問題とならない信号の配線に関しては、寄生容量を可能な限り小さくするため、その半導体集積回路装置内の最小配線幅に近い形成されている。あるいは、集積度の向上のため、最小配線幅および間隔をおくように配線が形成されている。

【０００４】また、配線層の厚さに関していえば、配線層を薄くすることは断面積を小さくすることとなり、電流密度を大きくすることになる。そうすると、エレクトロマイグレーションに対し悪くなるので、最小線幅が小さくなっても厚さが変らないようにしているのが現状である。

【０００５】

【発明が解決しようとする課題】図５はフォトレジスト３のパターニングした後の状態を示している。最近では、配線幅が０．６～０．８μｍ程度を用いるようになっているため、必然的にフォトレジスト３の幅が０．６～０．８μｍに対して、その厚さは配線層の厚さにより決定され、その厚さは１～３μｍ程度である。図５においては、０．８μｍの幅で２μｍの厚さの場合を例にとって示している。この様に、フォトレジスト３の断面形状は縦長状になっており、極端な場合には、配線層のエッチングを行うときにフォトレジスト３が倒れ、その下の配線層を残そうとしている部分までもがエッチングされてしまうといった問題点があった。

2

【０００６】この問題は配線パターンの直線部分が長いほど顕著であり、また図５に示すように、下層の２本の配線層８間と平行に配線層４を設けた場合に段差によりフォトレジストがどうしても厚くなってしまい、フォトレジスト３の断面形状は更に縦長状になってしまい、やはり問題が残ってしまう。

【０００７】これを防ぐには、配線幅を大きくしてフォトレジストが倒れないようにすればよいが、そうすると寄生容量が大きくなるといった問題が生じる。

【０００８】本発明は、上記従来技術の課題に鑑みて提案されたもので、半導体基板上に一方向に一定の幅で延在する配線が設けられた半導体集積回路において、配線に付く寄生容量の増大を最小限に抑制し、かつ、フォトレジストが倒れることを防止することを目的とする。

【０００９】

【課題を解決するための手段】本発明は、半導体基板上に一方向に一定の幅で延在する配線が設けられた半導体集積回路において、前記配線の一部に幅広部分を少なくとも一箇所設けることを特徴とする。

【００１０】

【作用】前記配線は全体としては配線幅は狭く設定されているので、寄生容量の増大を抑制でき、しかも、幅広部分の存在でフォトレジストが倒れるのが防止できる。

【００１１】

【実施例】本発明の第１実施例について説明する。図１は第１実施例の平面図であり、両側の配線パターン１の間に本発明の最小配線幅を用いた配線パターン２が２本存在する。これらの配線パターン２は夫々断面の幅が厚さの１．５～２倍程度の太さに設定されており、長さが数μｍに設定されている幅広部２０が所定の間隔をおいて形成されている。この幅広部２０の存在によりフォトレジストが倒れることが防止されるものである。

【００１２】上記第１実施例においては両最小線幅の配線パターン２に形成された幅広部２０が相互に向き合う位置に設けられていたが、第２実施例は図２に示すように、上下の最小線幅の配線パターン２に形成された幅広部を相互に長手方向にずらしては位置したものである。これにより両配線パターン２を接近させることができ、配線パターン２の間隔を狭めることが可能となる。

【００１３】

【発明の効果】上記したように本発明によれば、半導体基板上の一方向に一定の幅で延在する配線が設けられた半導体集積回路装置において、前記配線の一部に幅広部を設けることによって、配線の寄生容量の増大を最小限に抑制しながらもフォトレジストが倒れることを有効に防止することが可能となる。

【００１４】また、製造上のバラツキによりフォトレジストの残された幅が細くなってしまった場合においても、フォトレジストが倒れることを防止することが可能となる。

3

【図面の簡単な説明】

【図１】本発明の第１実施例を示した平面図。

【図２】本発明の第２実施例を示した平面図。

【図３】従来の配線を示した平面図。

【図４】従来の配線を示した断面図。

【図５】従来技術におけるフォトレジストのパターニン

4

グした後の状態を示した断面図。

【符号の説明】

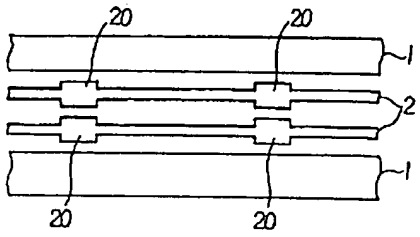
１…配線

２…本発明の配線

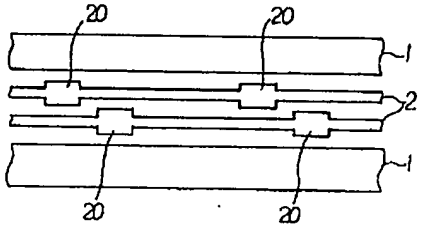
３…パターニング後のフォトレジスト

２０…幅広部

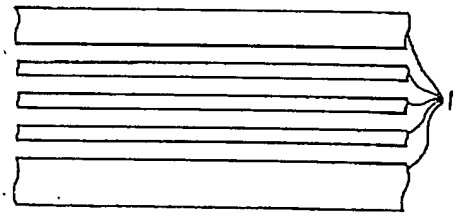
【図１】



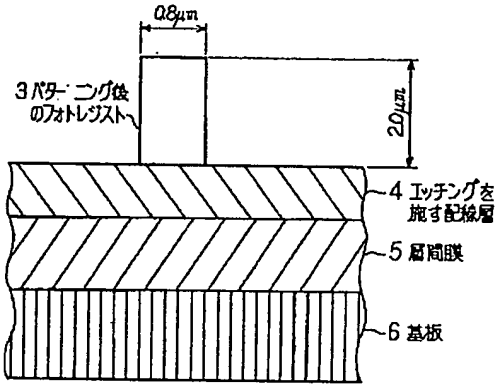
【図２】



【図３】



【図４】



【図５】